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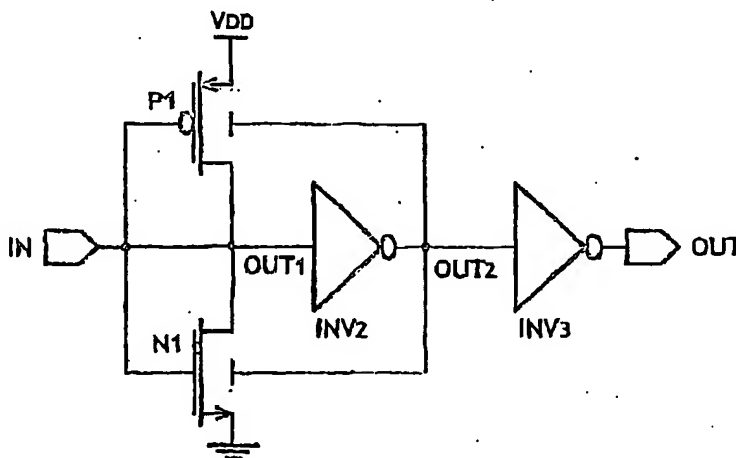
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[Continued on next page]

(54) Title: **SCHMITT TRIGGER CIRCUIT IN SOI**

(57) Abstract: This invention relates to a trigger circuit with hysteresis using the semiconductor on insulator technology, characterised in that it comprises at least two CMOS inverter stages, each inverter stage being composed of a first branch comprising at least one P-channel junction field effect transistor (PFET) in series between a first power supply potential VDD and an output node from the inverter stage, and a second branch comprising at least one N-channel junction field effect transistor (NFET) in series between the said output node from the inverter stage and a second power supply potential, the said transistors of each inverter stage having their grids connected together to receive an input signal, the input to each of the inverters directly or indirectly receiving the input signal of the said circuit, the output signal from the said circuit being obtained directly or indirectly by the output signal from one of the inverter stages and in that the substrate potential of each transistor of at least one inverter stage is dynamically controlled by a control signal output from the said circuit.

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INTERNATIONAL SEARCH REPORT

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6 239 649 B1 (BERTIN CLAUDE LOUIS ET AL) 29 May 2001 (2001-05-29) column 4, line 7 - line 34 column 5, line 47 - column 6, line 8 column 7, line 7 - line 40 figures 10,12,14	1-5,9, 16,17
Y	US 5 608 344 A (MARLOW C ALLEN) 4 March 1997 (1997-03-04) column 3, line 14 - column 4, line 26; figure 5	1-5,9, 16,17
A	US 6 441 663 B1 (CHUANG CHING-TE KENT ET AL) 27 August 2002 (2002-08-27) cited in the application column 3, line 58 - column 7, line 45; figures 3-11	1-17



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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US 6441663	B1	27-08-2002	NONE	